UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,246	04/06/2001	Makoto Terui	IIZ 122	7206

7590 08/26/2002

Steven M. Rabin
Rabin & Champagne, P.C.
Suite 500
1101 14th Street, N.W.
Washington, DC 20005

EXAMINER	
THAI, LUAN C	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/827,246	Applicant(s) TERUI ET AL.	
	Examiner Luan Thai	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse the embodiment of Species 19, as shown in Figures 40 and 41A-41B in Paper No. 5 is acknowledged. Claims 46-48 and newly added claims 49-61 read on the elected species.

Claims 1-45 have been canceled (paper No. 6).

Claims 46-48 and newly added claims 49-61 are pending in this application.

Information Disclosure Statement

2. The information disclosure statement (IDS) filed on 04/06/01 has been considered by the examiner.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Newly added claims **54-59** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim **58** is unclear since it depends on itself.

Claim **59** depends on claim **63**, which does not exist.

Claims **54-57** are rejected since each depends on claim **58**.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 46, 48-49, and 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takekawa et al (4,714,952).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 46 and 48-49, Takekawa et al disclose (see specifically figure 13) a semiconductor apparatus comprising: a substrate 74; a die pad 78 which comprises a second bonding area which is formed by extending outwardly all the sides of the die pad and where the conductor 82 is connected to; first terminals (G) and second terminals (P) being supplied with electrical power (Col. 17, lines 17+, and Col. 1, lines 13+); first conductive patterns 80' formed on the substrate and connected to the first terminals (G); second conductive patterns 80 formed on the substrate and connected to the second terminals (P); a ceramic layer of aluminum oxide or titanium oxide 54 (Col. 8, lines 1+) formed on the die pad 78; a metal layer 56 formed on the ceramic layer 54 and having a chip mounting area on which a semiconductor chip 36 is mounted and a first bonding area 56a surrounding the chip mounting area, the first bonding area being connected to the first conductive patterns 80' via wirings 90 and conductive posts 86. Although Takekawa et al do not explicitly disclose the first terminals (G) and the second terminal (P) being grounded and supplied with power, respectively, as claimed, such features are considered to be obvious in Takekawa et al device

structure since the first terminal (G) and the second terminal (P) appear to be terminals of a discrete capacitor having electrode plates 78-56 and being used in the device to eliminate the noises created between the electrical grounding and power of the source (Col. 17, lines 17+, and Col. 1, lines 13+).

Regarding claims 51-52, Takekawa et al further disclose the metal layer 56 having a shape to be smaller than the shape of the die pad 78 and partially covering the die pad.

6. Claims 47 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takekawa et al (4,714,952) in view of Wu et al (6,400,007).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 47 and 50, the proposed device structure of Takekawa et al discloses all the limitations of the claimed invention as detailed above except for a ridge surrounding the chip mounting area.

Wu et al while related to a similar semiconductor package design teach (see specifically figures 3-4) a ridge 52 surrounding the chip 28 for extending the overflow glue (Col. 3, lines 22+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Wu et al teachings to the proposed device structure of Takekawa et al by forming a ridge on the metal layer 56 and surrounding the chip 36 for controlling the over flow of the insulation layer 58 and thus, separating the chip mounting area from the ground bonding area.

7. Claims 53, 55-56, 58-59 and 60-61, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Takekawa et al (4,714,952) in view of Moriyama (5,962,917).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 53 and 55-56, the proposed device structure of Takekawa et al discloses all the limitations of the claimed invention as detailed above except for solder balls formed on the bond pads, which dispose on a lower surface of the substrate. (Note Takekawa et al disclose the conductors G/P extending from the sides to the lower surface of the substrate 74 to form the external terminals of the device package).

Moriyama while related to a similar semiconductor structure design teaches (see specifically figures 1-2) the external terminals of the device package can be conductors 33 extending from the sides to the lower surface of the substrate 31 (figure 1) or solder balls 46 formed on the ball mounting pads 45, which dispose on a lower surface of the substrate 41 and connected to the conductive patterns 42 via interconnecting patterns 11a (figure 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the proposed device structure of Takekawa et al by using solder balls and ball mounting pads formed on the lower surface of the substrate as external terminals of the device package, since such external terminals are conventional in the art as taught by Moriyama.

The further citations of claims 58-59 would have been obvious for the similar reasons set forth in the discussion of claims 51-52, respectively.

Regarding claims 60-61, the proposed device structure of Takekawa et al discloses all the limitations of the claimed invention as detailed above except for the substrate including an organic material.

A substrate making of either ceramic or an organic material, however, is conventional in semiconductor art as taught by Moriyama (Col. 5, lines 14+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate 74 in the proposed device structure of Takekawa et al of an organic material (instead of ceramic) since such material is conventional in semiconductor art as taught by Moriyama.

8. Claims 54 and 57, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Takekawa et al (4,714,952) in view of Moriyama (5,962,917) and further in view of Wu et al (6,400,007).

Regarding claims 54 and 57, the proposed device structure of Takekawa et al and Moriyama discloses all the limitations of the claimed invention as detailed above except for a ridge surrounding the chip mounting area.

Wu et al while related to a similar semiconductor package design teach (see specifically figures 3-4) a ridge 52 surrounding the chip 28 for extending the overflow glue (Col. 3, lines 22+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Wu et al's teachings to the proposed device structure of Takekawa et al and Moriyama by forming a

ridge on the metal layer 56 and surrounding the chip 36 for controlling the over flow of the insulation layer 58 and thus, separating the chip mounting area from the ground bonding area.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Albert W. Paladini 8-21-02

Luan Thai
August 19, 2002

ALBERT W. PALADINI
PRIMARY EXAMINER